Claims

I claim:

1. A communication system, comprising:

a transmitter, the transmitter coupled to receive N parallel bits of data and transmit the N parallel bits of data into K frequency separated channels on a transmission medium, where N and K are integers; and

a receiver coupled to receive data from the K frequency separated channels from the transmission medium and recover the N parallel bits of data.

2. The system of Claim 1, wherein the transmitter comprises

a bit allocation circuit that receives the N parallel bits of data and creates K subsets of data bits; and

K modulators, wherein each of the K modulators encodes one of the K subsets of the N parallel bits of data and creates an output signal modulated at a carrier frequency associated with one of the K frequency separated channels; and

an adder that receives the output signal from each of the K modulators and generates a transmit sum signal for transmission on the transmission medium

3. The system of Claim 2, wherein at least one of the K modulators includes

a data encoder that receives the one of the K subsets of the N parallel bits of data associated with the at least one of the K modulators and outputs an encoded signal;

a symbol mapper coupled to receive the encoded signal and output a symbol; and

an up-converter coupled to receive symbols from the symbol mapper and generate the output signal,

wherein the up-converter outputs data at the carrier frequency of one of the K frequency separate channels that corresponds with the at least one of the K modulators.

4. The system of Claim 3, further including a digital-to-analog converter coupled between the symbol mapper and the up-converter.

5. The system of Claim 3, wherein the data encoder is a trellis encoder.

6. The system of Claim 3, wherein the symbol mapper is a QAM symbol mapper which maps the encoded output signal into a symbol that includes an in-phase signal and a quadrature signal.

7. The system of Claim 4, further including a digital filter coupled between the symbol mapper and the digital-to-analog converter.

8. The system of Claim 4, further including a low-pass analog filter coupled between the digital-to-analog converter and the up-converter.

9. The system of Claim 6, wherein the up-converter generates a first signal by multiplying the in-phase portion of the complex symbol by a sine function of the carrier frequency, generates a second signal by multiplying the out-of-phase portion of the complex symbol by a cosine function of the carrier frequency, and summing the first signal with the second signal to generate the output signal.

10. The system of Claim 1, wherein the transmission medium is a copper backplane and the transmitter includes a differential output driver.

11. The system of Claim 1, wherein the transmission medium is FR4 copper trace and the transmitter includes a differential output driver.

12. The system of Claim 1, wherein the transmission medium is optical fiber and the transmitter includes an optical output driver.

13. The system of Claim 2, wherein a subset of bits at a lower carrier frequency contains fewer bits than a subset of bits associated with a higher carrier frequency.

14. The system of Claim 2, wherein each of the K subsets of data bits includes the same number of data bits.

15. The system of Claim 2, wherein the receiver comprises:

K demodulators, each of the K demodulators coupled to receive a signal from the transmission medium, the signal being the transmit sum signal transmitted through the transmission medium, and retrieving one of the K subsets of data bits; and

a bit parsing circuit that receives each of the K subsets of data bits from the K demodulators and reconstructs the N data bits transmitted by the transmitter.

16. The system of Claim 15, wherein the receiver further includes an input buffer coupled between the K demodulators and the transmission medium.

17. The system of Claim 16, wherein the input buffer receives a differential receive sum signal.

18. The system of Claim 16, wherein the input buffer receives an optical signal.

19. The system of Claim 15, wherein at least one of the K demodulators comprises:

a down-conversion circuit that receives the signal from the transmission medium and generates a symbol by converting the signal at the carrier frequency appropriate for the one of the K demodulators;

an equalizer circuit coupled to receive the symbol from the down-conversion circuit and create an equalized symbol; and

a decoder which receives the equalized symbol and retrieves the one of the K subsets of bits associated with the at least one of the K demodulators.

20. The system of Claim 19, further including an analog-to-digital converter coupled between the down-converter and the equalizer.

21. The system of Claim 20, further including an anti-aliasing filter coupled between the down-converter and the analog-to-digital converter.

22. The system of Claim 20, further including variable gain amplifiers coupled between the down-converter and the analog-to-digital converter, the variable gain amplifiers being controlled by an automatic gain circuit.

23. The system of Claim 19, wherein the symbol includes an in-phase signal and a quadrature signal and the down-converter multiplies the received sum signal by a cosine function to retrieve the in-phase component and by a sine function to retrieve the quadrature component.

24. The system of Claim 20, further including an adaptively controlled filter coupled between the digital-to-analog converter and the equalizer.

25. The system of Claim 24, further including a phase-rotator coupled between the adaptively controlled filter and the equalizer.

26. The system of Claim 19, wherein the equalizer parameters are adaptively chosen.

27. A method of communicating between components over a transmission medium, comprising:

separating N bits into K subsets of bits;

encoding each of the K subsets of bits to form encoded subsets of bits;

mapping each of the K encoded subsets of bits onto a symbol set to generate a K symbols representing each of the K subsets of bits;

up-converting each of the K symbols to form an up-converted signal at one of a set of K carrier frequencies;

summing the up-converted signals representing each of the K subsets of bits to generate a transmit sum signal; and

coupling the transmit sum signal to the transmission medium.

28. The method of Claim 27, wherein symbols transmitted at lower carrier frequencies represent fewer bits than symbols transmitted at higher carrier frequencies.

29. The method of Claim 27, wherein encoding each of the K subsets of bits includes encoding at least one of the K subsets of bits with a trellis encoder.

30. The method of Claim 27, wherein mapping each of the encoded subsets of bits includes QAM mapping.

31. The method of Claim 27, further including converting the K symbols to analog signals.

32. The method of Claim 31, further providing digital filtering prior to converting the K symbols to analog signals.

33. The method of Claim 31, further providing analog filter of the analog signals.

34. The method of Claim 27, further including

receiving a receive sum signal from the transmission medium;

down-converting the received sum signal into a set of K signals;

equalizing each of the K signals to receive equalized symbols;

decoding the equalized symbols to reconstruct the K subsets of bits; and

parsing K subsets of bits into N bits.

35. The method of Claim 34, wherein receiving the receive sum signal includes receiving a differential signal from a copper transport medium.

36. The method of Claim 34, wherein receiving the receive sum signal includes receiving an optical signal.

37. The method of Claim 34, wherein down-converting the received sum signal includes receiving a symbol transmitted at a corresponding carrier frequency.

38. The method of Claim 34, further including providing automatic gain conversion.

39. The method of Claim 34, further including providing analog-to-digital conversion.

40. The method of Claim 39, further including anti-aliasing filter prior to analog-to-digital conversion.

41. The method of Claim 34, further including providing adaptively controlled filtering for timing recovery.

42. The method of Claim 34, wherein the symbols are complex and further providing adaptively controlled phase rotation.

43. The method of Claim 34, wherein decoding the equalized symbols includes trellis decoding and QAM decoding.

44. A system for communication between components, comprising:

means for allocating N bits of input data into K subsets;

means for encoding each of the K subsets; and

means for transmitting each of the K subsets into one of K channels.

45. The system of Claim 44, further comprising:

means for receiving data from the K channels;

means for retrieving the K subsets; and

means for retrieving the N data bits.

46. A transceiver chip, comprising:

a transmitter portion, the transmitter portion coupled to receive N parallel bits of data and transmit the N parallel bits of data into a first set of K frequency separated channels on a transmission medium, where N and K are integers; and

a receiver portion coupled receive data from a second set of K frequency separated channels from the transmission medium and recover the N parallel bits of data.

47. The chip of Claim 46, wherein the first set of K frequency separated channels have substantially identical carrier frequencies with the second set of K frequency separated channels.

48. The chip of Claim 46, wherein the transmitter comprises:

a bit allocation circuit that receives the N parallel bits of data and creates K subsets of data bits; and

K modulators, wherein each of the K modulators encodes one of the K subsets of the N parallel bits of data and creates an output signal modulated at a carrier frequency associated with one of the first set of K frequency separated channels; and

an adder that receives the output signal from each of the K modulators and generates a transmit sum signal for transmission on the transmission medium

49. The chip of Claim 48, wherein at least one of the K modulators includes

a data encoder that receives the one of the K subsets of the N parallel bits of data associated with the at least one of the K modulators and outputs an encoded signal;

a symbol mapper coupled to receive the encoded signal and output a symbol; and

an up-converter coupled to receive symbols from the symbol mapper and generate the output signal,

wherein the up-converter outputs data at the carrier frequency of one of the K frequency separate channels that corresponds with the at least one of the K modulators.

50. The chip of Claim 49, wherein the encoder is a trellis encoder and the symbol mapper is a QAM symbol mapper.

51. The chip of Claim 46, wherein the receiver comprises:

K demodulators, each of the K demodulators coupled to receive a signal from the transmission medium, the signal being the transmit sum signal transmitted through the transmission medium, and retrieving one of the K subsets of data bits; and

a bit parsing circuit that receives each of the K subsets of data bits from the K demodulators and reconstructs the N data bits transmitted by the transmitter.

52. The chip of Claim 51, wherein at least one of the K demodulators comprises:

a down-conversion circuit that receives the signal from the transmission medium and generates a symbol by converting the signal at the carrier frequency appropriate for the one of the K demodulators;

an equalizer circuit coupled to receive the symbol from the down-conversion circuit and create an equalized symbol; and

a decoder which receives the equalized symbol and retrieves the one of the K subsets of bits associated with the at least one of the K demodulators.